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EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,594	JOHNSON, NEIL	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,18,20-24,26,27,33-35 and 37-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,18,20-24,26,27,33-35 and 37-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The instant application having application No. 10/679,594 has a total of 37 claims pending in the application; claims 1-15, 17, 19, 25, 28-32, and 36 have been canceled; claims 16, 23, and 33 have been amended; claims 38-51 have been added.

The indicated allowability of claims 19, 25, and 36, indicated in previous office action is withdrawn in view of the newly discovered reference(s). The Examiner would apologize if this causes any inconveniences. Rejections based on the newly cited reference(s) follow.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

Claims 38 and 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No 6,907,479 B2 to Karnstedt et al. (hereinafter Karnstedt).

1. In regard to claim 38 Karnstedt teaches:

"A data buffering unit **(e.g., Figs 2-3)**, comprising:"

"a memory that includes a plurality of first-in-first-out (FIFO) memories to store data;" **(e.g., FIFO Queues 208 in Fig. 2B; FIFO Queues Q0-Qmax in Fig. 3; column 7, lines 15-16).**

"a memory read manager to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device **(e.g., Read Control Logic 22 and Output MUX 170 in Fig. 2B)**, wherein the first data was prepared for output prior to a generation of the first read address **(e.g., column 10, lines 58-61; column 14, lines 13-19)**, and to prepare next data from a next storage element from the first FIFO memory for output by transmitting a read address to the first FIFO memory prior to a request for the next data from the data reading device." **(e.g., column 1, lines 31-34; column 20, lines 49-52).** *Karnstedt teaches a read pointer is incremented pointing to next subsequent location to be read on each of FIFO read access. On one embodiment Karnstedt teaches that parameter comprising next FIFO read location stored in a register file. Therefore, the data is prepared in prior to transmitting an address from the reading device.*

2. *In regard to claim 40 Karnstedt teaches:*

"wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading device." **(e.g., column 11, lines 7-9; element 170 in Fig. 1).**

3. *In regard to claim 41 Karnstedt teaches:*

"wherein the memory read manager comprises a read selector **(e.g., element 170 in Figs. 1 and 2B)**, coupled to data outputs of each of the FIFO memories **(e.g., arrow between FIFO Queues 208 and MUX 170)**, to select an appropriate data output to receive data from in response to a read address from the data reading device." **(e.g., column 5, lines 2-5; MUX 170 in Fig. 1).**

4. In regard to claim 42 Karnstedt teaches:

"wherein the memory read manager comprises a plurality of read pointer managers, each corresponding to one of the FIFO memories **(e.g., Read Pointers 224 in Fig. 2B)**, the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device." **(e.g., column 1, lines 31-34; column 20, lines 49-52).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 16, 18, 20-21, 23-24, 26-7,33-35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5, 867,727 to Hattori in view of U.S. Patent No. 5,557,750 to Moore et al. (hereinafter Moore) and U.S. Patent No. 6,615,296 B2 to Daniel et al. (hereinafter Daniel).

5. In regard to claim 16, Hattori teaches:

"A method for managing data," **(e.g., see claim 16))** comprising:"

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device," **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.17).** *For example the address bits A7 to A5 coincide with the bits set in the FIFO is selected and the oldest (e.g., first data-in) data or first data is read out. However, Hattori does not expressly teach:* "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device; and preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device."

Moore teaches: "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device;" **(e.g., see column 7, lines 66-67 to column 8, lines 1-3; Fig. 2)** *For preparing the next data for prefetching within a clock cycle.*

Daniel teaches: "preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.." **(e.g., see column 5, lines 63-64)** *For providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the next location within the FIFO to be read.*

Disclosures by Moore, Hattori, and Daniel are analogous because all references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system taught by Hattori to include prefetching disclosed by Moore furthermore to include the read pointer taught by Daniel.

The motivation for using prefetching data as taught by column 2, lines 4-7 of the Moore is to allow data to be available within one clock cycle, eliminating host waiting for an internal data bus cycle. By thus eliminating host-waiting state, overall system performance is significantly enhanced. Furthermore, the motivation for using RP as taught by column 5, lines 62-63 of Daniel is to reduce the number of access required. This reduction would significantly increase FIFO throughput.

Therefore, it would have been obvious to combined teaching of Daniel and Moore with Hattori to obtain the invention as specified in the claim.

6. *In regard to claims 18 and 35 Moore teaches:*

"wherein the first data is output within a clock cycle after the first read address from the data reading device is generated." **(e.g., see column 7, lines 23-24; and lines 66-67 to column 8, lines 1-4; Fig. 2).**

7. *In regard to claims 20 and 26 Hattori teaches:*

"selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).** *Hattori teaches that first FIFO 38-1 and second FIFO 38-*

2 can be selected for reading by providing address bits 31 to 5 to decoding circuit 70 (e.g., see Fig. 15). Address 7 to 5 to select 1 of the 8 FIFOs 38-1 to 38-2. The control processors provide addresses A31 to A5 to decoding circuits for reading data from any of the 8 FIFOs. However, Hattori does not expressly teach: "preparing next data from a next storage element from the second FIFO memory for output."

Moore teaches: "preparing next data from a next storage element from the second FIFO memory for output." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).**

8. *In regard to claims 21, 27, and 37 Hattori teaches:* selecting any of plurality of 8 FIFOs for data output but does not expressly teaches: "... preparing of the next data from the next storage element ..."

Moore teaches: "... preparing of the next data from the next storage element ..." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).**

9. *In regard to claim 23, Hattori teaches:*

"A method for managing data **(e.g., see claim 16)**, comprising:"

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device," **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.17).** *For example the address bits A7 to A5 coincide with the bits set in the FIFO is selected and the oldest (e.g., first data-in) data or first data is read out. However, Hattori does not expressly teach:* "wherein the first data is output within a

clock cycle after the first read address is generated; and preparing next data from a next storage element from the first FIFO memory for output."

Moore teaches: "wherein the first data is output within a clock cycle after the first read address is generated;" **(column 7, lines 23-24; and lines 66-67 to column 8, lines 1-4; Fig. 2).**

Daniel teaches: "preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.." **(e.g., see column 5, lines 63-64)** *For providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the next location within the FIFO to be read. The motivation for combining is based on the same rational given in claim 16.*

10. In regard to claims 24 and 34 Moore teaches:

"wherein the first data was prepared for output by the first FIFO memory prior to a generation of the read address from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).** *For example data is prepared and stored in prefetch register prior to next Bus cycle (e.g., prior to generation or read address).*

11. In regard to claim 33, Hattori teaches:

"A method for managing data **(e.g., see claim 16)**, *comprising:"*

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories **(e.g., elements 38-1 to 38-8 in Fig. 12)** *to output first data stored in a first storage element in*

the first FIFO memory in response to a first read address from a data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).**

"selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).** *Hattori teaches that first FIFO 38-1 and second FIFO 38-2 can be selected for reading by providing address bits 31 to 5 to decoding circuit 70 (e.g., see Fig. 15). Address 7 to 5 to select 1 of the 8 FIFOs 38-1 to 38-2. The control processors provide addresses A31 to A5 to decoding circuits for reading data from any of the 8 FIFOs. However, Hattori does not expressly teach: "preparing next data from a next storage element from the second FIFO memory for output."*

Moore teaches: "preparing next data from a next storage element from the second FIFO memory for output..." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).** *For example preparing data to be ready in prefetch register.*

Daniel teaches: "...by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.." **(e.g., see column 5, lines 63-64)** *for providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the next location within the FIFO to be read. The motivation for combining is based on the same rational given in claim 16.*

Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori in view of Moore and Daniel as applied to claim16 above, and further in view of U.S. Patent Publication 2002/0152263 A1 to Goldrian et al. (hereinafter Goldrian).

12. In regard to claim 22, the Hattori in view of Moore and Daniel teach all limitations recited in claim 16 but does not expressly teach: "writing data into the plurality of FIFO memories in a round robin fashion."

Goldrian teaches: "writing data into the plurality of FIFO memories in a round robin fashion." **(e.g., see paragraph 71 in page 4)** *for writing to FIFOs in a round-robin fashion.*

Disclosures by Hattori, Moore, Daniel and Goldrian are analogous because all references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system and method taught by Hattori, Moore, Daniel to include writing to FIFOs in round-robin fashion taught by Goldrian.

The motivation for using round-robin as taught by paragraph 58, page 3 of Goldrian is to keep the packet sequence in order.

Therefore, it would have been obvious to combined teaching of Goldrian, Moore, Daniel, and with Hattori to obtain the invention as specified in the claim.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karnstedt in view of U.S. Patent 6,304,936 B1 to Sherlock.

13. In regard to claim 39 Karnstedt teaches all limitations included in claim 38 but does not expressly teach: "wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories."

Sherlock teaches*:* "wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories." **(e.g., see column 8, lines 58-64; column 11, lines 57-65; elements 100 and 1325 in Fig. 13)** *for applying read enable signal to each FIFO.*

Disclosures by Karnstedt and Sherlock are analogous both references teach methods of implementing and managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to include the read enable to FIFO devices taught by Sherlock.

The motivation for including read enable as taught by column 1, lines 7-10 of the Sherlock is to include FIFO buffers in a bus bridge to improve bandwidth efficiency and reduce circuits size and cost.

Therefore, it would have been obvious to include teachings of Sherlock with Karnstedt to obtain the invention as specified in the claim.

Claims 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karnstedt in view of Goldrian.

14. In regard to claim 43 Karnstedt teaches:

"further comprising a memory write manager that directs data from the data transmitting device to be written into each of the FIFO memories ..." **(e.g., Write Control Logic 212**

in Fig. 2A). *However, Karnstedt does not expressly teach: "...writing data into the plurality of FIFO memories in a round robin fashion."*

Goldrian teaches: "...writing data into the plurality of FIFO memories in a round robin fashion." **(e.g., see paragraph 71 in page 4)** *for writing to FIFOs in a round-robin fashion.*

Disclosures by Karnstedt and Goldrian are analogous both references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system and method taught by Karnstedt to include writing to FIFOs in round-robin fashion taught by Goldrian.

The motivation for using round-robin as taught by paragraph 58, page 3 of Goldrian is to keep the packet sequence in order.

Therefore, it would have been obvious to combined teaching of Goldrian with Karnstedt to obtain the invention as specified in the claim.

15. In regard to claim 44 Karnstedt teaches:

"wherein the memory write manager comprises a write address manager that determines which of the FIFO memories to access in response to a write address received from the data transmitting device." **(e.g., see column 1, lines 27-29; Write Control Logic 212 in Fig. 2A).**

16. In regard to claim 45 Karnstedt teaches:

"wherein the write address manager determines a write address in one of the FIFO memories to write data in response to the write address received from the data

transmitting device." **(e.g., see column 10, lines 24-25; Write Control Logic 212 in Fig. 2A).**

17. In regard to claim 46 Karnstedt teaches:

"wherein the memory write manager comprises a write selector that transmits a write enable signal and data from the data transmitting device to an appropriate FIFO memory in response to the work address manager." **(e.g., see column 9, lines 65 to column 10, line 1).**

Claims 47 and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karnstedt in view of U.S. Patent No. 6,891,397 B1 to Brebner.

18. In regard to claim 47 Karnstedt teaches:

"memory blocks that form comprise a plurality of first-in-first-out (FIFO) memories **(e.g., FIFO Queues Q0-Qmax in Fig. 1)** to store data from a data transmitting device;" **(e.g., see column 4, lines 66 to column 5, lines 1-2).**

"logic elements to form a memory read manager to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device **(e.g., Read Control Logic 22 and Output MUX 170 in Fig. 2B)**, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device **(e.g., column 10, lines 58-61; column 14, lines 13-19)**, and to prepare next data from a next storage element from the first FIFO memory for output by transmitting a read address to the first FIFO memory prior to a request for the next data from the data reading device." **(e.g.,**

column 1, lines 31-34; column 20, lines 49-52). *However, Karnstedt does not expressly teach:* "A programmable logic device (PLD)..."

Brebner teaches: "A programmable logic device (PLD)..." **(e.g., see column 2, lines 22-24; column 7, lines 44-46; elements 326-1 to 326-4)** *for using PLD to implement logic and memory functions including FIFO buffers.*

Disclosures by Karnstedt and Brebner are analogous both references teach methods of implementing and managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to include the PLD system disclosed by Berbner FIFO devices taught by Karnstedt.

The motivation for including PLD as taught by column 1, lines 36-37 of the Brebner is to implement a system-level integration for flexibility and efficiency.

Therefore, it would have been obvious to include teachings of Brebner with Karnstedt to obtain the invention as specified in the claim.

19. In regard to claim 49 Karnstedt teaches:

"wherein the memory read manager comprises a read address manager to determine which of the plurality of FIFO memories to access in response to a read address from the data reading device." **(e.g., column 11, lines 7-9; element 170 in Fig. 1).**

20. In regard to claim 50 Karnstedt teaches:

"wherein the memory read manager comprises a read selector **(e.g., element 170 in Figs. 1 and 2B)**, coupled to data outputs of each of the FIFO memories **(e.g., arrow between FIFO Queues 208 and MUX 170)**, to select an appropriate data output to

receive data from in response to a read address from the data reading device." **(e.g., column 5, lines 2-5; MUX 170 in Fig. 1).**

21. In regard to claim 51 Karnstedt teaches:

"wherein the memory read manager comprises a plurality of read pointer managers, each corresponding to one of the FIFO memories **(e.g., Read Pointers 224 in Fig. 2B)**, the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device." **(e.g., column 1, lines 31-34; column 20, lines 49-52).**

Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karnstedt in view of Brebner as applied to claim 47 above, and further in view of Sherlock.

22. In regard to claim 48 Karnstedt in view of Brebner teaches all limitations include in claim 47 but does not expressly teach: "wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories."

Shelock teaches: "wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories."

(e.g., see column 8, lines 58-64; column 11, lines 57-65; elements 100 and 1325 in Fig. 13) *for applying read enable signals to each FIFO.*

Disclosures by Sherlock, Brebner, and Karnstedt are analogous both references teach methods of implementing and managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to include the read enable to FIFO devices taught by Sherlock furthermore to include PLD as taught by Brebner.

The motivation for including read enable as taught by column 1, lines 8-10 of the Sherlock is to FIFO buffers in a bus bridge to improve bandwidth efficiency and reduce circuits size and cost. Furthermore, the motivation for using PLD as taught by column 1, lines 36-37 of the Brebner is to implement a system-level integration for flexibility and efficiency.

Therefore, it would have been obvious to include teachings of Sherlock and Brebner with Karnstedt to obtain the invention as specified in the claim.

Response to Applicant Remarks

It has been noted that Applicant has amended some of the claims and has added new claims to include the allowable subject matters indicated in the previous Office Action. However, as stated above, in view of newly discovered reference(s) the indicated allowability of claims are withdrawn. The Examiner would apologize if this causes any inconveniences.

Conclusion

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

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2006-10-11

Brian R. Peugh
Primary Examiner